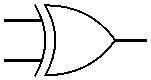
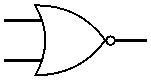
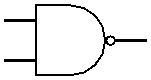
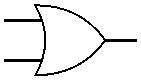
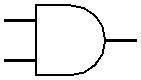
Lab 1: Digital Logic Gates and Boolean Functions

# Data Sheet

## Introduction to Basic Logic Gates



### Figure F.1.1: Pin configurations of gates in ICs

|  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- |
| **Input** | **AND** | **OR** | **NAND**  ̅̅̅ ̅̅ ̅ | **XOR** | **NOR**  ̅ ̅̅ ̅̅̅̅ ̅ |  | **Input** | **NOT**  ̅ |
| 0 0 | 0 | 0 | 1 | 0 | 1 | 0 | 1 |
| 0 1 | 0 | 1 | 1 | 1 | 0 | 1 | 0 |
| 1 0 | 0 | 1 | 1 | 1 | 0 |  | | |
| 1 1 | 1 | 1 | 0 | 0 | 0 |

**Table F.1.1: Truth Table of Logic Gates**

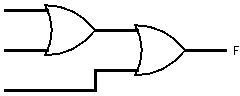
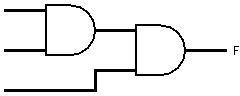
* 1. **Constructing 3-input AND & OR gates from 2-input AND & OR gates**

|  |  |  |
| --- | --- | --- |
| A B C | F = ABC | F = A+B+C |
| 0 0 0 | 0 | 0 |
| 0 0 1 | 0 | 1 |
| 0 1 0 | 0 | 1 |
| 0 1 1 | 0 | 1 |
| 1 0 0 | 0 | 1 |
| 1 0 1 | 0 | 1 |
| 1 1 0 | 0 | 1 |
| 1 1 1 | 1 | 1 |

**Table F.2.1: Truth Tables for 3-input AND and OR**

|  |
| --- |
| F = ABC = A(BC) = (AB)C |
| F = A+B+C =A+(B+C) =(A+B)+C |

**Table F.2.2: Expressing 3-input gates as 2-input gates using associative law.**

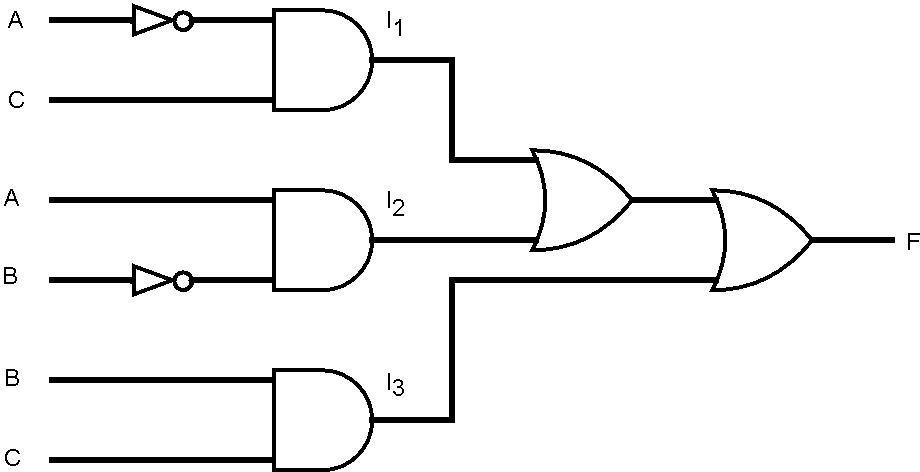


**Figure F.2.1: Extension of inputs of AND and OR gates**

* 1. **Implementation of Boolean Functions**

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| A B C | I1 = A’C | I2 = AB’ | I3 = BC | F= I1+ I2 + I3 |
| 0 0 0 | 0 | 0 | 0 | 0 |
| 0 0 1 | 1 | 0 | 0 | 1 |
| 0 1 0 | 0 | 0 | 0 | 0 |
| 0 1 1 | 1 | 0 | 1 | 1 |
| 1 0 0 | 0 | 1 | 0 | 1 |
| 1 0 1 | 0 | 1 | 0 | 1 |
| 1 1 0 | 0 | 0 | 0 | 0 |
| 1 1 1 | 0 | 0 | 1 | 1 |

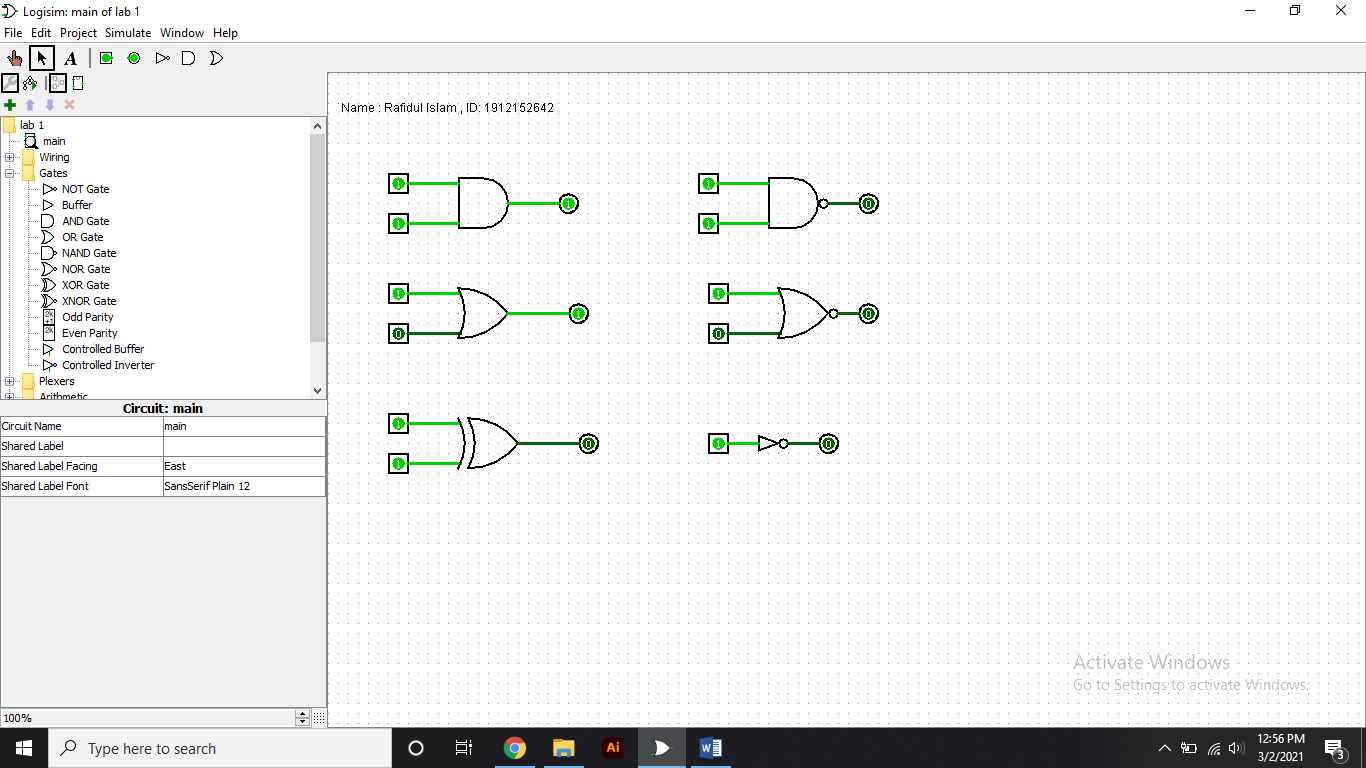
**Figure F.3.1: Truth Table for the given Boolean Function**



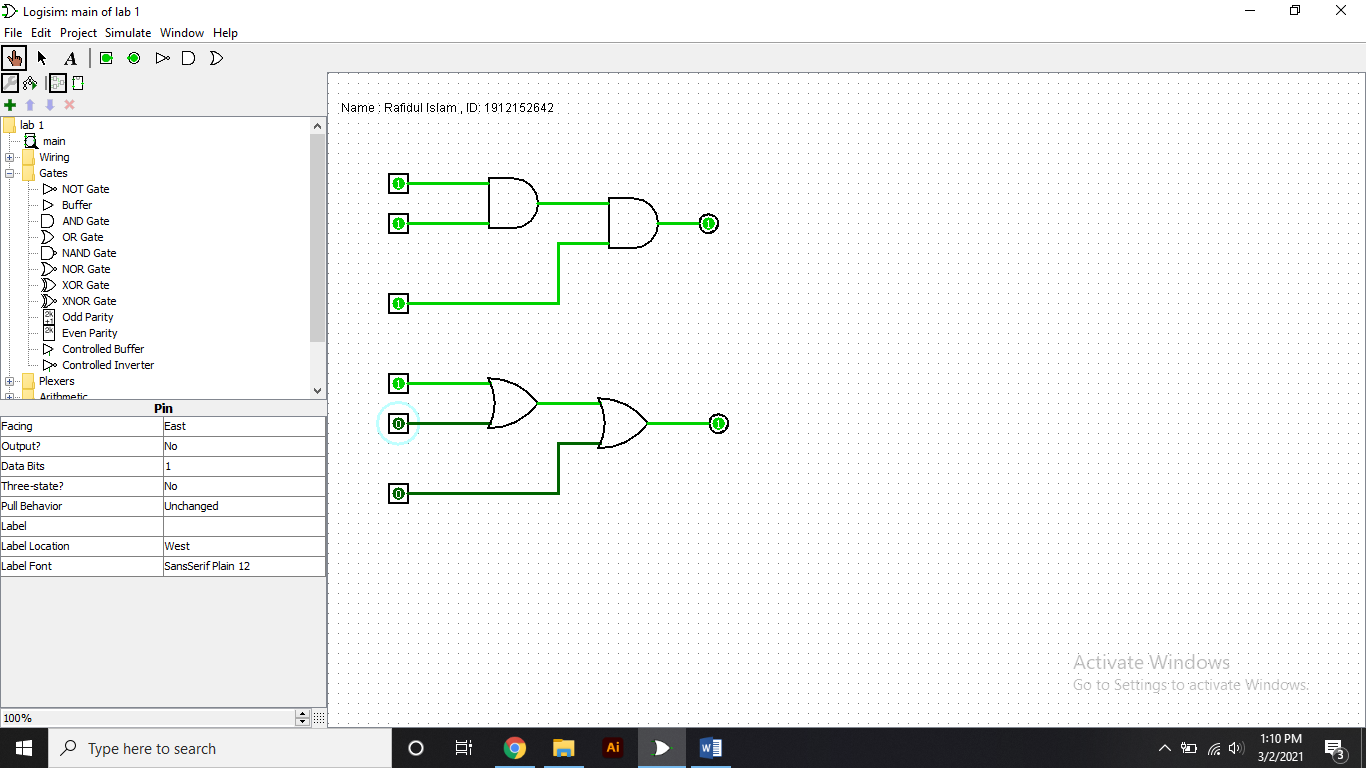
**Figure F.3.1: Logic Diagram for the given Boolean Function**

**Attachment:**

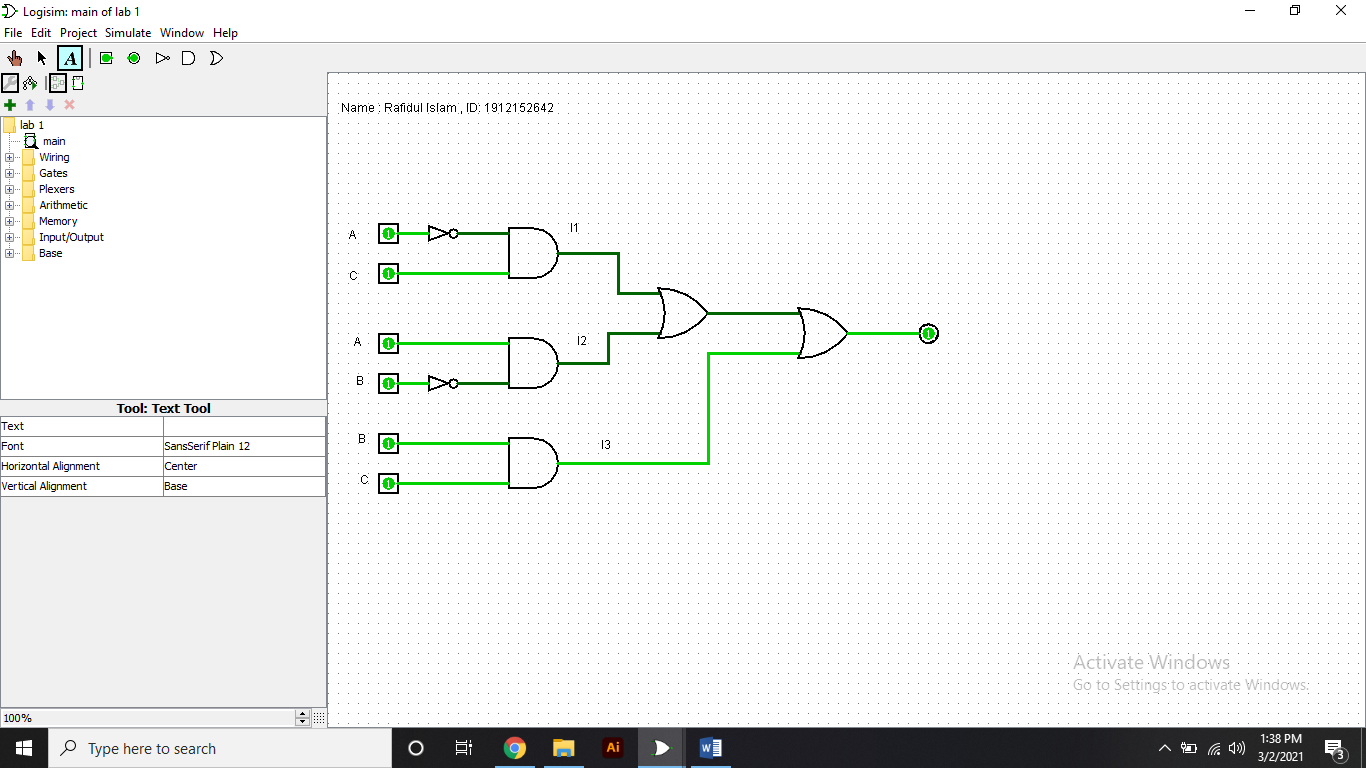
1. Attach the screenshots /image of the simulations below
2. Attach the required logic Diagrams with proper figure name and labeling below.



**F.1.1**



**F.2.1**



**F.3.1**